Combination of InP MZM Transmitter and Monolithic CMOS 8-State MLSE Receiver for Dispersion Tolerant 10 Gb/s Transmission

Robert A. Griffin[1], **Norman Swenson**[2], **Diego Crivelli**[2], **Hugo Carrer**[2],
Mario Hueda[2], **Paul Voois**[2], **Oscar Agazzi**[2], **Fabricio Donadio**[2]

[1]Bookham, Inc., Caswell, Towcester NN12 8EQ, UK, , [2]ClariPhy Communications, Inc., 16 Technology Drive, Suite 165, Irvine, CA 92618 USA
[1]robert.griffin@bookham.com, [2]norm.swenson@clariphy.com

Abstract: We demonstrate that InP modulators together with 1 sample/bit MLSE gives equivalent performance to linear electro-optic Mach-Zehnder modulators combined with oversampled MLSE, potentially providing significant reduction in power dissipation and footprint.

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1. Introduction

Maximum Likelihood Sequence Estimation (MLSE) is a powerful technique for post-receiver mitigation against chromatic and polarization-mode dispersion in single-mode fiber transmission [1]. For application in long-haul optical networks requiring tunability and tolerance to ASE noise, previous studies of MLSE performance have employed lithium-niobate Mach-Zehnder modulators ($LiNbO_3$ MZMs). However, small size and low drive voltage requirements make alternative InP-based MZMs very attractive for transponder and transceiver applications. Here we study the combination of InP MZMs with a novel monolithic CMOS 8-state MLSE chip operating at 10.7 Gb/s. We consider both noise-loaded and receiver power-limited regimes, with performance measured over 300 km of SMF-28 fiber (5000 ps/nm dispersion) with a 1 sample/bit MLSE architecture.

2. InP MZMs

Whereas $LiNbO_3$ MZMs utilize the linear electro-optic (Pockel's) effect, InP MZMs exploit 'electro-refractive' effects. The devices studied here employ an MQW structure, grown with band-edge ~ 150nm below the operating wavelength. Reverse bias results in large absorption changes due to the QCSE, which in turn translates to refractive index change at the operating wavelength via the Kramers-Kronig relation. The relatively large electro-refractive effects enable electrode interaction lengths ~ 10x smaller than linear electro-optic MZMs. A consequence of utilizing the electro-refractive effect is that the induced optical phase change is slightly nonlinear; additionally, there is residual voltage-dependent absorption. While the impact of these effects is small for zero-chirp transmission up to ~ +/-1000ps/nm with conventional clock and data recovery, here we investigate performance for considerably longer spans enabled by the use of MLSE following the photodetector.

Figure 1 shows a schematic of the MQW InP MZM design [2]. The MZM uses 1.5 mm length lumped-element electrodes on a deeply-etched ridge waveguides having P-i-N doped epitaxial layers. The undoped MQW core of the MZM waveguide consists of 31 periods of lattice-matched InGaAsP wells and InGaAsP barriers. The InP MZM is co-packaged together with a full-band tunable digital-supermode distributed Bragg reflector (DS-DBR) laser, in a compact module with industry-standard 14-pin footprint (30mm×12.7mm). Both laser and MZM are mounted on thermo-electric coolers (TECs), ensuring high stability. Coplanar feed-throughs are used for DC laser and modulator connections, and a coplanar GSGSG arrangement is used for the RF modulation path. An Al_2O_3 carrier for the InP MZ with terminated 50Ω coplanar transmission lines allows independent drive signals for each modulator arm. Differential modulation is compatible with low-cost SiGe or GaAs driver ICs, which provide ~5Vpp differential drive with low power consumption.

3. CMOS MLSE Chip

Figure 2 shows a simplified block diagram of the MLSE receiver. Unlike previously reported implementations of MLSE, which were multi-chip modules with SiGe front-end analog-to-digital converters (ADCs) [3,4], the MLSE chip employed here is a single CMOS die. Power dissipation for the current chip is ~ 4.5 Watts. The availability of advanced volume silicon process technology is expected to further reduce power dissipation for the monolithic CMOS MLSE chip to well below that of existing multi-chip SiGe/CMOS implementations, enabling wider application for MLSE technology in optical links.

The CMOS chip monolithically integrates the programmable gain front end amplifier (PGA), ADC, timing recovery, automatic gain control (AGC), feed-forward equalizer (FFE), channel estimator, and Viterbi decoder. Realizing the 10 Gsample/s ADC in standard CMOS required a novel 8-way interleaved architecture using open-loop amplifiers and look-up table calibration [5]. To our knowledge, the current chip is the first 10G MLSE solution to incorporate an FFE, a multi-input/multi-output (MIMO) parallel structure implementing 25 T-spaced taps [6]. The length of the equalizer is selectable in 5-tap increments, allowing one to trade performance for power consumption. The MLSE algorithm implements a sliding block Viterbi decoder (SBVD) with a selectable number of states, either 4 or 8. The channel estimator includes Volterra modeling to compensate nonlinear channel effects.

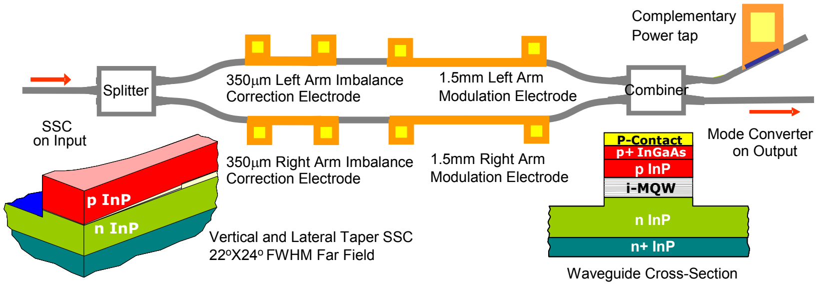


Fig. 1. InP MZM layout and waveguide structure

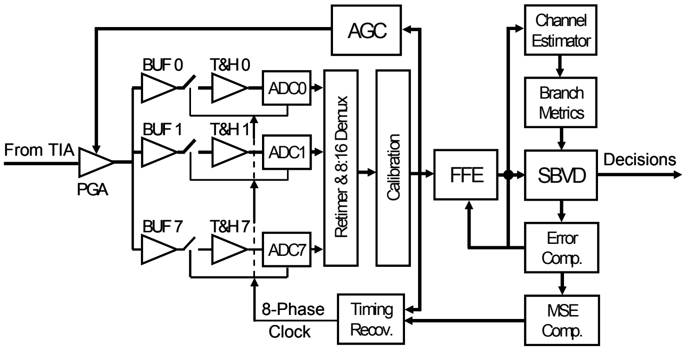


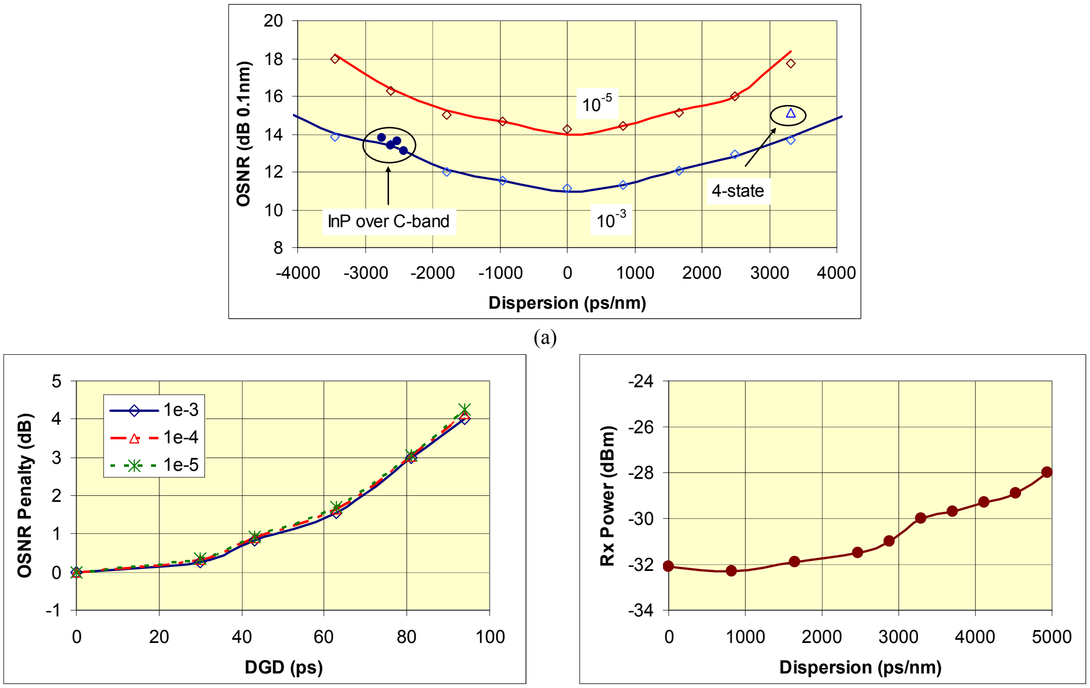
Fig. 2. Simplified block diagram of MLSE receiver.

4. Results

For chromatic dispersion measurements, the optical signal was launched over consecutive spans of SMF-28 or DCF, with EDFA stages compensating loss. Noise loading was performed at the end of the span with an unpolarized ASE source, and signal OSNR measured with an OSA. An optical bandpass filter preceded the receiver, which was an APD-TIA combination. For 1^{st}-order PMD measurements, several lengths of characterized PMF were used with a manual polarization controller at the input. The input SOP was adjusted for worst-case performance with equal power in fast and slow axes. BER measurements (pre-FEC) were performed at 10.7 Gb/s, using a 2^{31}-1 PRBS sequence from a pattern generator. For each measurement, the MLSE chip performed blind adaptation, providing serial output data which was analyzed with an error detector.

As a reference measurement, an X-cut $LiNbO_3$ MZM with 1550nm source laser was employed as the transmitter. With all other parts of the link constant, a zero-chirp InP-based transmitter and driver IC was substituted. As shown in Fig. 3a, excellent dispersion tolerance was achieved using 8-state MLSE, with ~ 3dB OSNR variation covering +/-3000 ps/nm of dispersion. With the chip configured for 4-state MLSE, performance was degraded by ~ 2dB at 200 km distance. The performance of niobate and InP MZMs were closely overlaid; several data points measured around −2500 ps/nm show little variation with wavelength for the InP MZM over C-band. Despite the different physics that underlie the realization of modulation for the alternative MZMs, there is little impact for signal recovery over the longer spans enabled by MLSE detection. In all cases, results compare favourably with MLSE performance from an oversampling approach [1]. We attribute the excellent performance measured here for the 1-sample/bit architecture to the combination of FFE preceding MLSE detection and the use of 8 states. Performance measurement against 1^{st}-order PMD, shown in Fig. 3b, also demonstrates results comparable to oversampled MLSE [7].

The availability of powerful FEC and advanced components for dispersion mitigation with low power, small footprint, and fullband tunability provides new opportunities for application in metropolitan-area networks, spanning distances up to several hundred kilometres. To test performance in this regime, a negative-chirp InP MZM was used together with the MLSE receiver, operating at an OSNR of 25dB over SMF-28 fiber. For each span length, the receiver power was reduced, degrading BER until the target 10^{-4} value was reached. As shown in Fig. 3c, performance degraded gracefully over an uncompensated span of 300 km (~5000 ps/nm dispersion).



(a)

(b)

(c)

Fig. 3. a) Required OSNR for given BER with $LiNbO_3$ (open symbols) and InP MZMs (solid curves); b) OSNR penalty with 1st-order PMD; c) Receiver sensitivity for 10^{-4} BER at 25dB OSNR.

4. Summary

Performance of a monolithic CMOS MLSE chip was evaluated together with an InP MZM-based transmitter at 10.7 Gb/s. Excellent tolerance to chromatic and polarization-mode dispersion was measured, with results comparable to alternative approaches using oversampled ADCs and linear electro-optic modulators. The compact size and low power dissipation of the InP and CMOS combination offers great potential for significant size reduction of existing approaches, opening new possibilities for transponder and transceiver applications.

5. References

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