

## Overview

**Position:** Senior ASIC DFT Engineer

**Reporting to:** Director, Silicon Implementation

**Location:** Irvine, CA or Los Altos, CA

## Job Description

The engineer will be responsible for the DFT implementation, design, coding, synthesis and static timing analysis of the next general optical networking ASICs. Typical activities include development of hardware block design specifications, RTL coding, synthesis, formal verification (LEC), static timing analysis and DFT design implementation/ATPG/verification. The engineer will interface with the backend group for the physical implementation of these hardware blocks. He or she will also be expected to contribute to development of effective full chip/block DFT methodology.

## Required Skills & Experience

- Must be able to develop best in class, highest quality DFT methodologies to meet all test requirements & silicon quality standards
- Must drive DFT tools to produce highest quality DFT implementation for both core design as well as integration of IPs.
- Must drive ATPG tools to meet all silicon coverage requirements.
- Must work well with RTL design, test engineering teams to implement highest quality DFT implementation.
- Will have verification responsibilities of chip design for all DFT requirements, including DFT functional verification, DFT coverage verification in all DFT modes.
- Static Timing/Noise/Coupling Analysis related to all DFT modes or ATPG
- Must be able to generate clear documentation & easy to use scripts in support DFT flows.
- Must be capable of driving evaluation of tools in the development of DFT flows.
- Hands on experience with the following areas:
  - Logic Bist, Memory Bist, Boundary Scan, scan/ATPG design implementation & verification
  - DFT process/flow development experience
  - Understanding of static timing and crosstalk/noise analysis.
  - Understanding of synthesis/timing closure concepts.
  - Write and read RTL in Verilog and/or VHDL.
  - Coding in scripting languages such as TCL, Perl and UNIX shell.
- Hands on experience with following EDA tools:
- DFT: DFT Compiler/MAX, LogicVision\*, TetraMAX, Fastscan, TestKompress
- Lint: Spyglass\*, NLINT
- Synthesis: Design Compiler\*
- Static timing: Primetime\*
- \* indicates the preferred tools
- Experience with low power DFT flows highly desirable
- Bachelor's in Engineering or equivalent required

For more information, please visit our website [www.clariphy.com](http://www.clariphy.com) or contact us at [careers@clariphy.com](mailto:careers@clariphy.com).

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