

# Architecture and Experimental Evaluation of a 10Gb/s MLSD-Based Transceiver for Multimode Optical Fibers

Diego Crivelli\*, Hugo Carrer\*, Mario Hueda\*, Norman Swenson, Paul Voois, Oscar Agazzi  
ClariPhy Communications, Inc.

16 Technology Drive, Suite 165 Irvine, CA, 92618, U.S.A.

\*Digital Communications Research Laboratory - National University of Córdoba - CONICET

Av. Vélez Sarsfield 1611 - Córdoba (X5016GCA) - Argentina

{dcrivelli, hscarrer, mhueda}@ieee.org, {norm.swenson, paul.voois, oscar.agazzi}@clariphy.com

**Abstract**— In this paper we present the architecture and experimental evaluation of a single-chip CMOS maximum-likelihood sequence detection (MLSD) transceiver for electronic dispersion compensation (EDC) of multimode optical fibers (MMF) at 10Gb/s data rate. The primary application of this transceiver is the 10GBASE-LRM standard for 10Gb/s Ethernet over MMF [1]. Application to single-mode fiber (SMF) channels and/or other standards is also possible. Both optical module and line card applications are discussed. The architecture of the receiver is discussed in considerable depth, including implementation details. Extensive experimental results on several channels are presented. For the precursor, postcursor, and symmetric stressors specified by the 10GBASE-LRM standard we demonstrate receiver sensitivities of -14.84dBm, -14.37dBm, and -13.68dBm, respectively, in a line card application with 6 inches of electrical interconnect. These sensitivities exceed the requirements of the standard by 8.34dBo, 7.87dBo, and 7.68dBo<sup>1</sup>, respectively. Measured results on industry defined worst-case fibers and on nonstationary channels such as the dynamic stressor defined by the 10GBASE-LRM standard are also presented.

## I. INTRODUCTION

Maximum-likelihood sequence detection (MLSD) has attracted considerable interest in recent literature as an electronic dispersion compensation (EDC) technique for single mode optical fibers (SMF), particularly for long-haul or metropolitan area network applications [2], [3], [4]. However, most of the literature on EDC for multimode fibers (MMF) is based on the decision-feedback equalizer [5], [6]. The MMF channel differs significantly from the SMF channel, therefore the application of MLSD to MMF requires new work. Although some of the recent literature [7], [8] studies this problem from a theoretical point of view, experimental results have not been reported so far. To the best of the authors knowledge, the transceiver reported in this paper is the first MLSD based EDC transceiver for the MMF channel.

Multimode fibers are typically used in local area network (LAN) applications, in links whose length could reach or exceed 300 meters. A large percentage of the existing fiber population consists of legacy fibers that exhibit large multimode

<sup>1</sup>dBo stands for optical decibel.

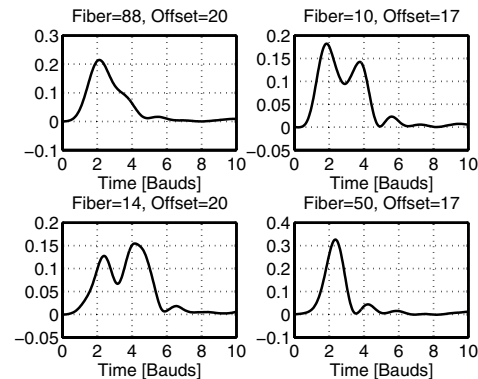


Fig. 1. Typical MMF impulse responses

dispersion. Interest in EDC for MMF has grown significantly in recent years as a result of the standardization activities of the IEEE 802.3aq Task Force, which developed the 10GBASE-LRM standard [1] for 10 Gb/s Ethernet over MMF, based on the application of EDC technology. Fig.1 shows some typical MMF impulse responses, taken from one of the databases used by the IEEE 802.3aq Task Force, known as the Cambridge database [9]. The dispersion is caused by the difference in propagation velocities of the different modes. By contrast, the dominant forms of dispersion in SMF are chromatic (CD) and polarization-mode dispersion (PMD). In general, both the time span of the impulse responses and the variability of their shapes make equalization of MMF more difficult than that of SMF. For example, some recently proposed MLSD receivers for SMF do not include a Feedforward Equalizer (FFE). This may be motivated by the difficulty of implementing the FFE at 10 Gb/s data rate. While this may be acceptable in SMF applications, it would cause an unacceptable performance loss on multimode channels. This is experimentally demonstrated in Section IV.

It is interesting to mention that the response of some MMF may be nonstationary (this is also true for PMD in SMF). Other impairments of the MMF channel include relative intensity noise (RIN), modal noise (MN), and thermal noise.

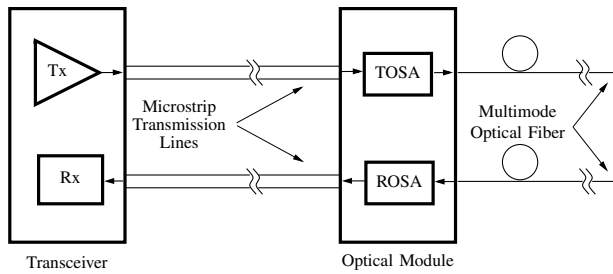


Fig. 2. Simplified model of the optical and electrical channels. TOSA stands for Transmit Optical Sub Assembly, and ROSA stands for Receive Optical Sub Assembly. In addition to the transmission lines, the electrical channel may include connectors, chip pads, and other components.

These will be discussed in the next section. In addition to the intrinsic channel impairments, the optical receiver may have to cope with implementation-related impairments. In this paper, we present a digital signal processing (DSP) implementation for the MLSD receiver, where the only analog blocks are those that provide an interface with the external world. The most important of them is the input analog to digital converter (ADC). We present a thorough experimental evaluation of the performance of this receiver.

The rest of this paper is organized as follows. In Section II we describe the MMF channel and discuss some of the challenges it presents to the receiver. In Section III we describe the transceiver architecture including implementation considerations. In Section IV we present measurement results. Finally, in Section V we draw conclusions.

## II. THE MULTIMODE FIBER CHANNEL

Throughout this paper, we use the channel proposed by the 10GBASE-LRM standard [1] as the primary example of application of the proposed techniques. The transmitter uses a 1310nm Fabry-Perot or DFB laser. Light can be launched into the MMF using either center or offset launch conditions [10]. The launch condition can have a dramatic impact on the response of the fiber. At the receive end, the optical signal is detected by a PIN photodiode and the photocurrent is converted to a voltage and amplified using a transimpedance amplifier (TIA) and a linear post amplifier. Legacy MMFs suffer from significant modal dispersion. On some MMFs, particularly under center launch conditions, the response may vary over time as a result of vibrations or mechanical stress on the fiber [11], [12].

Noise in MMF links is dominated by RIN, MN, and thermal noise [13]. While RIN and MN are nongaussian, thermal noise, mainly produced by the TIA at the input of the receiver, is Gaussian. Nonlinearity may be introduced in the signal by the laser and/or the TIA and post amplifier. In many applications, the transceiver is located inside an optical module. Therefore the channel described above constitutes the entire channel over which the transceiver is expected to operate. However, interest has developed in recent years in a communication equipment configuration in which the transceiver is mounted on a printed circuit board (often called the *line card*) outside the optical module. The requirements for this configuration are given

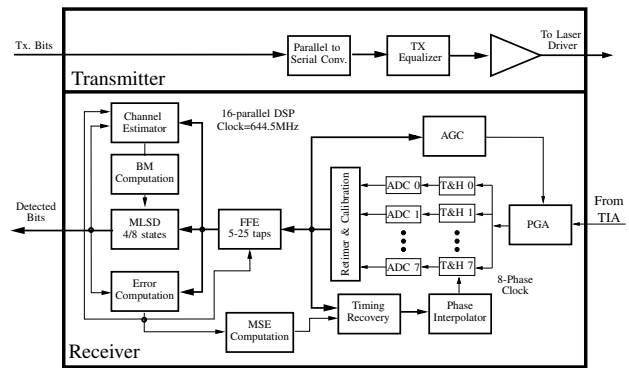


Fig. 3. Transceiver Block Diagram.

by the SFP+ Specification [14]. The interconnection between the optical module and the transceiver involves components such as microstrip transmission lines, connectors, and others. Fig. 2 shows a simplified diagram. See [14] for a detailed description of the electrical channel. There are important practical advantages in this configuration, for example the fact that the optical module is considerably simplified and, consequently, its cost is reduced. Also, this configuration lends itself well to taking advantage of the advances in VLSI technology, because it enables the integration of multiple transceivers on a single chip and/or the integration of the physical layer transceiver with protocol control engines. In a line card configuration, the electrical channel adds significant attenuation and dispersion to those contributed by the optical channel, and therefore it must be taken into account in the design of the transceiver. Performance evaluation done in a line card configuration (Section IV) provides a lower bound for the transceiver performance in a module configuration.

## III. TRANSCEIVER ARCHITECTURE

In this section we describe the transceiver architecture. Fig. 3 shows a simplified block diagram. On the transmit path, the data is transmitted serially through the transmit buffer, which drives an external laser driver directly (in a module application) or through the electrical transmit path (in a line card application). Intersymbol interference (ISI) generated by the electrical transmit path is transformed into data dependent jitter (DDJ) by the laser driver, which is essentially a limiting amplifier that slices the input signal at a certain threshold. To reduce DDJ, the transmitter must precompensate for the ISI introduced by the transmit path. This is accomplished by a 10-tap programmable transversal equalizer. The taps are implemented using digitally programmable current sources. The equalizer is divided into two sections. The first section consists of seven contiguous taps (a main tap, three precursor and three postcursor taps). The second section, consisting of three taps, is separated from the first one by a programmable delay varying between 0 and 40 bit periods. This second section is intended to equalize the reflection at the far end of the electrical channel, which results from imperfect match-

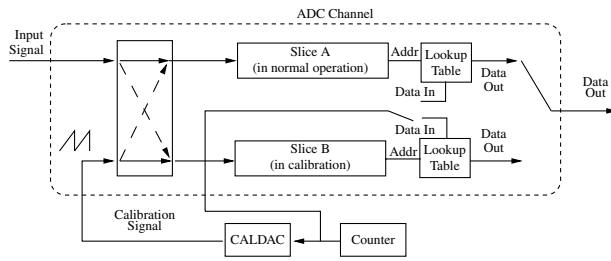


Fig. 4. Simplified diagram of the ADC calibration scheme

ing of the termination. In the receive path, the dispersion introduced by the electrical channel in a line card application is combined with the dispersion of the optical channel. The equalizer can compensate for both. However, the task of the equalizer becomes significantly more challenging as a result of the presence of the electrical channel. The level of the input signal is adjusted by a programmable gain amplifier (PGA), whose gain is controlled by a digital automatic gain control (AGC). The PGA consists of a coarse and a fine section. The coarse section is a passive attenuator with eight settings and attenuations between 0dB and 17.5dB, in steps of 2.5dB. The fine section is an amplifier with a gain between 0 and 14dB. The coarse PGA is set during the startup and remains fixed afterwards. The fine PGA is continuously adapted, and its main function is to absorb dynamic variations of the received optical power. The fine PGA gain is controlled digitally with an 8 bit control word. The output of the PGA is applied to an array of eight interleaved track and hold (T&H) amplifiers, followed by eight ADCs. The T&H amplifiers take samples of the input signal at a rate of 1289.0625Ms/s each, but the sampling clocks of the different interleaves are staggered in phase by 96.97ps, so that the signal is sampled at an aggregate rate of 10.3125Gs/s. This is also the symbol rate in the LRM channel, therefore the receiver samples the signal at the symbol rate. Mismatches across the eight interleaves in the sampling phase, gain, or frequency response of the T&H amplifiers and/or the ADCs can cause a performance degradation known

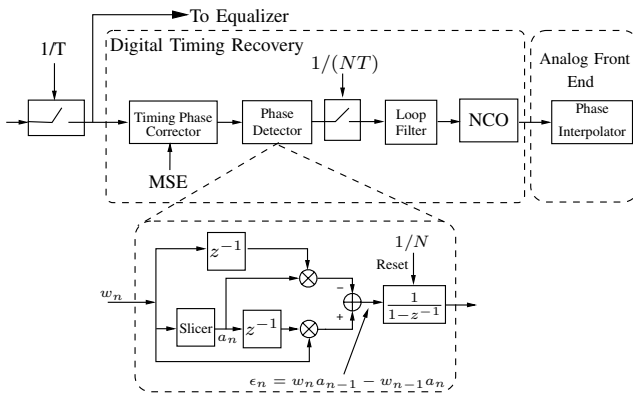


Fig. 5. Timing recovery block diagram

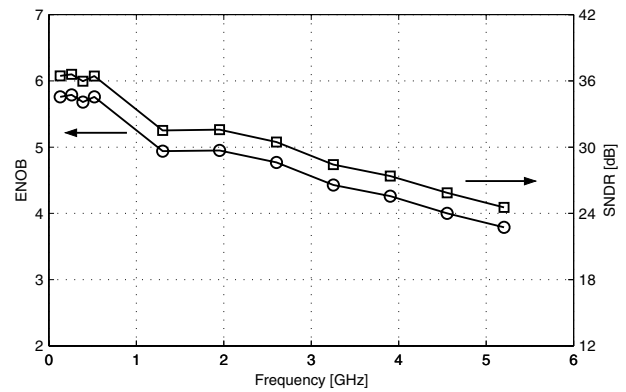


Fig. 6. Measured ENOB and SNDR as functions of frequency for the calibrated ADC.

as fixed pattern noise. MIMO equalization techniques are used to compensate this impairment. A brief discussion of these techniques is presented below. A more thorough discussion can be found in [15]. The outputs of the eight interleaved ADCs are further demultiplexed by a factor 2, retimed to a single 644.5312MHz clock, and passed to the DSP-based receiver, which uses a parallel processing architecture with a parallelization factor of 16. Digital calibration is used to compensate for the nonlinearity of the ADCs. A background calibration scheme is used (Fig. 4). Each one of the eight interleaved ADC channels mentioned before actually consists of two identical 10-bit pipelined ADCs (called ADC slices) and a calibration lookup table implemented in a RAM. At any given time, one of the slices is in normal operation, and the other is in calibration. Calibration is accomplished by feeding the input of the slice under calibration with a linear ramp generated by a 10-bit DAC (called the CALDAC). The lookup table is adapted using the pipelined ADC output as the RAM address, and the CALDAC input code as the expected value. During normal operation, the lookup table is used to correct the raw codes generated by the ADC. The two slices of any given ADC channel are constantly switching back and forth between calibration mode and normal operation, but this is transparent to the outside world, that sees the combination of the two slices and their respective lookup tables and output multiplexer as a single ideal ADC. Although for simplicity clock boundaries are not shown in Fig. 4, calibration takes place in the DSP clock domain, after retiming and demultiplexing. Because each ADC generates two samples per DSP clock cycle, dual-port RAMs are used to implement the lookup tables. The calibrated output of the ADCs has 8 bit nominal resolution, and 5.8 effective number of bits (ENOB) at low frequency. Fig. 6 shows the measured signal to noise plus distortion ratio (SNDR) and the measured ENOB as functions of frequency.

The AGC is based on a parallel-processing peak detector with fast attack and slow release characteristics. This results in good tracking of changes in the signal amplitude and robustness to impulsive noise. Fig. 5 is a simplified block

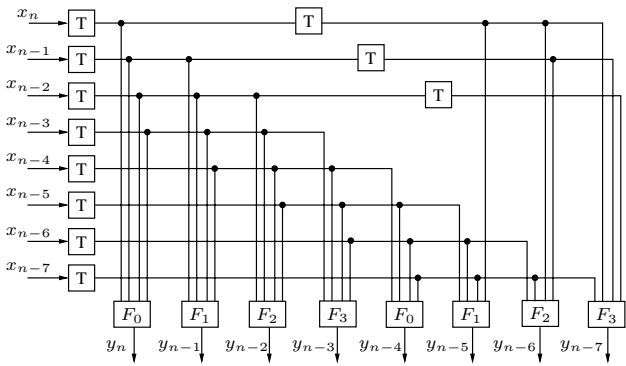


Fig. 7. Example of 4-tap, 8-parallel MIMO FFE. The actual implementation is 25-tap, 16-parallel. Processing elements  $F_k$  are 25-tap FIR filters, where coefficients for different  $k$  are independent.

diagram of the Timing Recovery block. The signal, sampled at the baud rate, is passed through a first-order all-pass filter that introduces a variable delay, and then passed to the phase detector, which is based on a modified Mueller and Muller [16] algorithm, where pseudo decisions, instead of true decisions, are used to compute the timing function. This is done to reduce latency in the feedback loop. Pseudo decisions are simply the result of slicing the unequalized signal. An outer control loop monitors the receiver mean squared error (MSE) and adjusts the programmable delay of the all-pass filter, seeking to minimize the MSE. Thus, the receiver can change the sampling phase chosen by the Timing Recovery block and optimize the signal to noise ratio (SNR). Notice that the delay introduced by the all-pass filter affects only the signal entering the Timing Recovery block.

The main stages of the receiver are a 25-tap MIMO FFE, and the 8-state Viterbi decoder. The MIMO FFE (Fig. 7) uses a 16-parallel architecture with eight independent sets of coefficients, corresponding to the eight channels of the AFE. The 25-tap processing elements  $F$  of Fig. 7 are FIR filters built using five distributed arithmetic sections of five taps each. These sections can be deactivated and powered down to trade power dissipation for performance, making the effective length of the filter a programmable parameter between 5 and 25 taps, in steps of 5. For similar reasons, the number of states of the Viterbi decoder can be reduced to 4 by a configuration bit. The Viterbi decoder is based on a sliding block architecture [17].

At each clock cycle, a block of 32 samples is input to the decoder. The 32-sample block is formed by concatenating the 16 most recent samples of the FFE output with the 16 previous. The Viterbi decoder uses 16 samples for initialization of the path metrics, and releases 16 bits at each clock cycle. The branch metrics are computed using lookup tables addressed by the samples of the input signal. For each branch in the trellis, the table contents are based on the output of a MIMO nonlinear channel estimator (Fig. 8) based on a Volterra series expansion, with a maximum memory of four bit periods. The MIMO architecture used in the FFE and the channel estimator compensates differences in the channel response across the eight

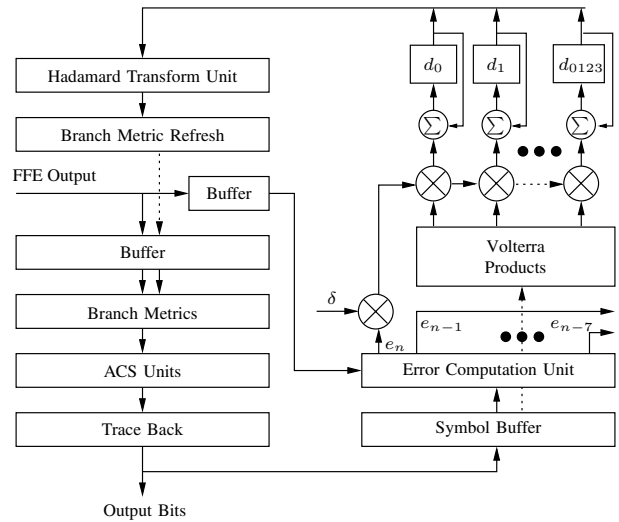


Fig. 8. Viterbi decoder and channel estimator

interleaves of the analog front end (AFE). These differences arise from mismatches in the gain, sampling phase, offset, and frequency response of the AFE channels [15]. The FFE and the channel estimator are adapted jointly using the LMS algorithm. The coefficients of the FFE are processed by the lookup table refresh unit, which computes the contents of the lookup tables used in the distributed arithmetic implementation of the FFE. Similarly, the Volterra coefficients of the channel estimator are postprocessed by the Hadamard transform unit to compute the contents of the branch metric lookup tables. Besides the analog front end and signal processing functions just described, the receiver incorporates functions such as the physical coding sublayer (PCS) specified by [18], clause 49, a XAUI interface ([18], clause 47), as well as blocks dedicated to testing and channel monitoring. The complete transceiver is implemented as a single chip in 90nm CMOS technology, with an area of 32mm<sup>2</sup>. Fig. 9 shows a chip photo.

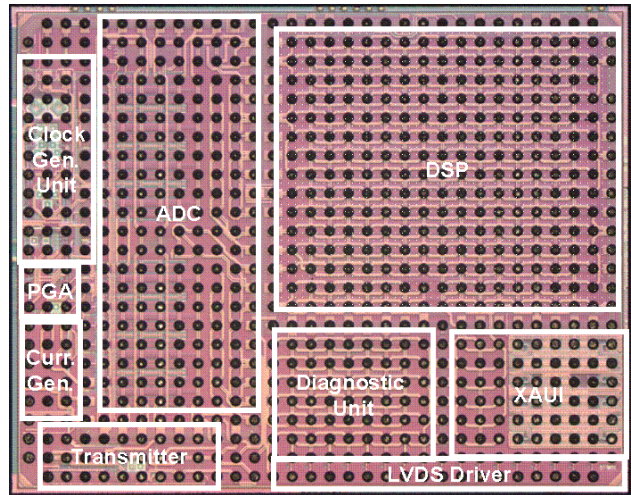


Fig. 9. Chip photo

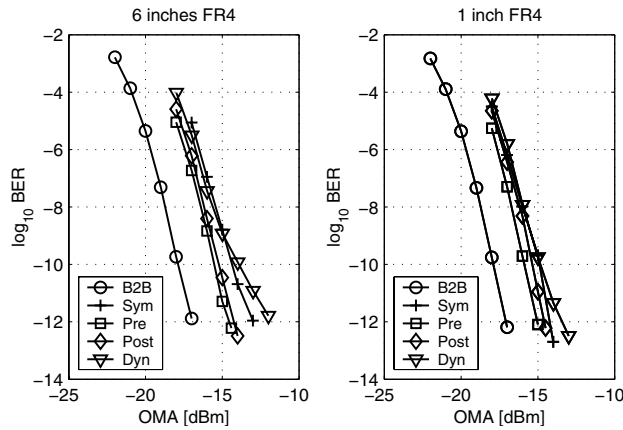


Fig. 10. Measured chip performance in a line card configuration where the length of the electrical channel is 6 (left) and 1 (right) inches.

TABLE I  
RECEIVER SENSITIVITIES AND MARGINS OVER REQUIREMENTS OF THE 10GBASE-LRM STANDARD

Stressor	6 in.		1 in.	
	Sens. [dBm]	Margin [dBo]	Sens. [dBm]	Margin [dBo]
B2B	-17.5	11	-17.27	10.77
Pre	-14.84	8.34	-15.36	8.86
Post	-14.37	7.87	-14.74	8.24
Sym	-13.68	7.68	-14.34	8.34
Dyn	-12.61	6.11	-13.67	7.17

#### IV. EXPERIMENTAL RESULTS

In this section we present comprehensive experimental results obtained in laboratory measurements of the transceiver. The measurements were done in a line card configuration, using a Hydra LRM tester from Circadian Corporation. The optical module used was a Sumitomo Electric Industries SPP510ILM-GL. Curves of bit error rate (BER) versus optical modulation amplitude (OMA) were plotted for the transceiver described in this paper using the precursor, postcursor, and split symmetric stressors defined by the 10G BASE-LRM standard [1], as well as the dynamic stressor provided by the Hydra tester. The frequency of oscillation of the latter was 10Hz. For comparison purposes, the curve corresponding to a back to back configuration is also shown. In Fig. 10 we show the resulting curves for a line card configuration where the length of the electrical channel is 6 (left) and 1 (right) inches. The receiver sensitivity is defined as the value of OMA for which the BER is  $10^{-12}$ . From these curves, the sensitivities of the receiver when operating with the IEEE stressors are determined. These sensitivities are shown on Table I for the precursor, postcursor, split symmetric and dynamic stressor, together with the margins over the requirement of the standard. The large margins observed are a dramatic demonstration of the benefit of the MLSD architecture and the DSP-based implementation.

In Fig. 11 we show the BER curves for the industry standard round-robin fibers [19]. The length of these fibers is 300m. Both center launch and offset launch conditions are used.

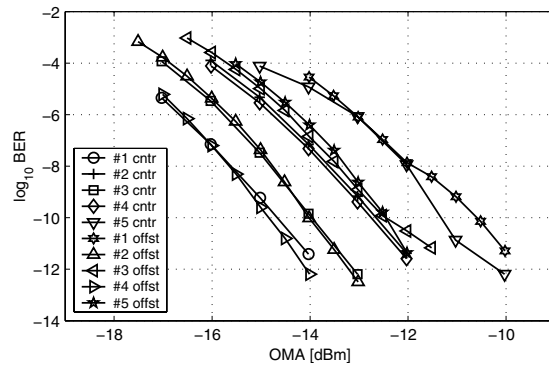


Fig. 11. Measured chip performance with round robin fibers, the length of the electrical channel is 1 inch.

Fig. 12 illustrates the measured impulse response for one of the fibers under both center and offset launch conditions. A measure of the difficulty of the channel is given by the value of the receive waveform dispersion penalty (RWDP). This quantity is similar to the Transmit Waveform and Dispersion Penalty (TWDP) defined in the 10GBASE-LRM standard [18] (see also [20]), but it is applied to the received waveform. From Section 68.6.9.3 of [1], the precursor, symmetrical, and postcursor stressors used to test compliance have RWDP values of 4.1, 3.9, and 4.2dBo, respectively. The RWDP values for 10 channels are tabulated in Table II, together with the measured receiver sensitivities. From the table, we see that some of the measured channels have RWDP values that significantly exceed those of the IEEE stressors, which implies they are significantly harder, yet the receiver sensitivity exceeds the requirement of Table 68-5 of the standard by a large amount. In the particular case of fiber No.3 and offset launch conditions, the sensitivity is -11.75dBm in spite of the fact that the RWDP value is 7.2dBo. This is another dramatic demonstration of the robustness of the architecture proposed in this paper.

As mentioned in the Introduction, some recently proposed receivers for single-mode fiber applications use a Viterbi decoder but not an FFE. As shown by Forney [21], the optimal MLSD receiver requires a whitened matched filter, which in practice is approximated by an input low-pass filter followed by the FFE. While not using an FFE may be appropriate for SMF applications, it would result in an unacceptable degradation on MMF channels. Figure 13 shows measurements illustrating this effect when the channel is the IEEE LRM symmetric stressor. The (1/4) and (1/8) configurations correspond to a 4 and an 8 state Viterbi decoder, respectively, with a 1-tap FFE (which is equivalent to no FFE). For these configurations, the receiver displays a BER floor at approximately  $10^{-6}$  and  $10^{-8}$ , respectively.

#### V. CONCLUSIONS

We have presented the architecture of a new single chip MLSD-based optical transceiver implemented in 90nm CMOS technology, and the results of its laboratory characterization.

TABLE II  
RWDP VALUES AND SENSITIVITIES FOR THE 10 ROUND-ROBIN  
CHANNELS UNDER TEST

Fiber	RWDP [dBo]	Sens. [dBm]
#1 cntr	2.7	-13.9
#2 cntr	5.4	-12
#3 cntr	2.6	-13.26
#4 cntr	3.7	-12.05
#5 cntr	5.1	-10.29
#1 offst	5.0	-9.9
#2 offst	3.8	-13.38
#3 offst	7.2	-11.75
#4 offst	3.0	-14.17
#5 offst	6.2	-11.94

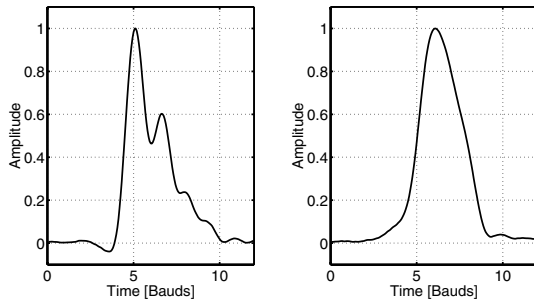


Fig. 12. Impulse responses of round robin channels for cases #5 cntr (left) and #5 offst (right)

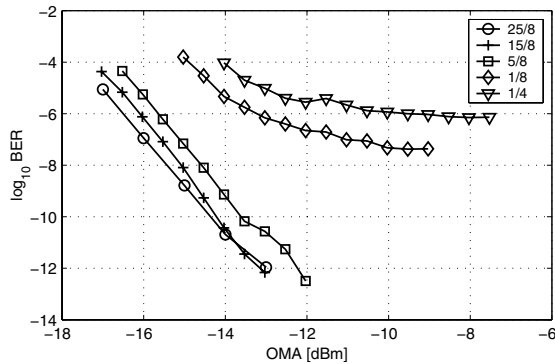


Fig. 13. FFE impact on system performance for LRM symmetric stressor (number of FFE taps/number of MLSD states).

The primary application of this transceiver is electronic dispersion compensation in multimode fiber optical communications, although other applications are also possible, including communications on single-mode fibers. The architecture of the transceiver has been described in detail, and extensive measurement results have been presented. Measurements show that the transceiver exceeds the requirements of the 10GBASE-LRM standard by a large margin.

Finally, the receiver operates reliably on the Telecommunications Industry Association round-robin fibers. Measures of the challenge presented by these fibers and the receiver performance when operating on them are given in Table II.

## ACKNOWLEDGEMENTS

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