Overview

ClariPhy Communications' CL1012 MLSE-based EDC+Repeater device is a 9.95 - 11.4 Gb/s repeater / retimer IC combining the Clock and Data Recovery (CDR) function with high-speed Digital Signal Processing (DSP) required for Electronic Dispersion Compensation (EDC). The applications supported include multi-mode fiber links at transmission distances up to 300 m as well as single-mode fiber links at transmission distances beyond 400 km. The advanced MLSE-based EDC function enables the CL1012 to overcome the impairments of the fiber channel, optical front end, and electrical interconnect. Functional blocks include Maximum Likelihood Sequence Estimation (MLSE), Feed Forward Equalization (FFE) Transmit Pre-emphasis, and Clock and Data Recovery (CDR).

Key Features

- Universal CDR with built-in EDC for metro, and long-haul SONET/SDH and DWDM applications
- Single-chip CMOS with integrated ADC and DSP
- 16-tap FFE and 8-state MLSE
- Operates at data rates from 9.95 to 11.4 Gb/s
- Offset threshold adjustment for ASE noise
- Built-in pattern generators (PRBS9/31) and BER detectors
- On board channel diagnostics
- MDIO and I^2C Management Interfaces
- 10x10 mm^2, 144-Lead PBGA Package

Major Benefits

- All-digital MLSE-based EDC offers robust compensation of CD, PMD and nonlinearities
- Small footprint for 300 pin, XFPe, XFP MSA applications
- Integrated CMOS implementation behaves reliability and robustly across voltage and temperature
- DSP-based timing recovery and adaptation guarantees predictable and consistent convergence
- DSP provides multiple diagnostic and self-test features

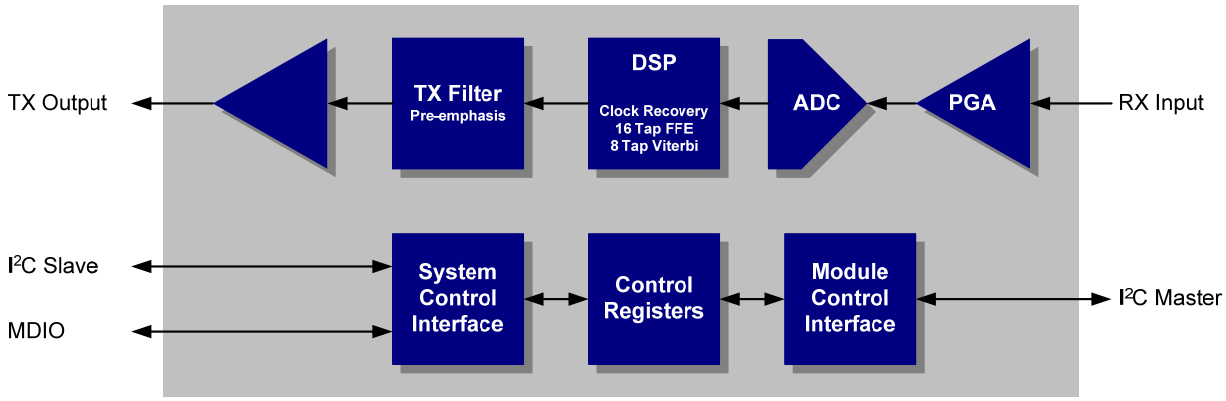

Figure 1, Functional Diagram

Product Description

ClariPhy Communications' CL1012 all-digital, CMOS, MLSE-based EDC Repeater is a 9.95-11.4 Gb/s physical layer (PHY) IC integrating high-speed digital signal processing (DSP) for advanced Electronic Dispersion Compensation (EDC), and clock and data recovery / repeating functionality. The applications targeted include multi-mode fiber links at transmission distances up to 300 m as well as single-mode fiber links at transmission distances from 10km to beyond 400 km. The advanced MLSE-based EDC function enables the CL1012 to overcome the impairments of the fiber channel, optical front end, and electrical interconnect. Functional blocks include Maximum Likelihood Sequence Estimation (MLSE), Feed Forward Equalization (FFE) Transmit Pre-emphasis, and Clock and Data Recovery (CDR). The CL1012 chip is designed for use with existing 10G-base SR and LR, emerging Ethernet 802.3aq Long Range Multimode (LRM), 10G SONET, and short-reach copper cabling applications.

In the receive path, the CL1012 receives the serial data directly from the Trans-impedance Amplifier (TIA) and digitizes it to a 16-bit word format. An FFE and MLSE decoder compensates for dispersion that occurs in the fiber-optic channel, as well as distortion introduced by the electrical interconnect between the CL1012 and the optical front end. The serial transmit path offers a filtered (with pre-emphasis) and a straight differential output option.

The device includes both an MDIO and a system two wire Interface (I^2C) to provide access to the CL1012 internal registers for configuration and management. The choice of management interface is user selectable. A second I^2C is also used as a bridge between the system controller and an optical module, allowing the host controller to request control and status information for the optical module.

The CL1012 device operates from a 1.0 V digital core voltage and a 1.8 V analog voltage. The digital I/O signals are 3.3 V tolerant. A highly flexible architecture allows the CL1012 to be configured to accommodate varying application scenarios and power modes.

CL1012 Block Diagram

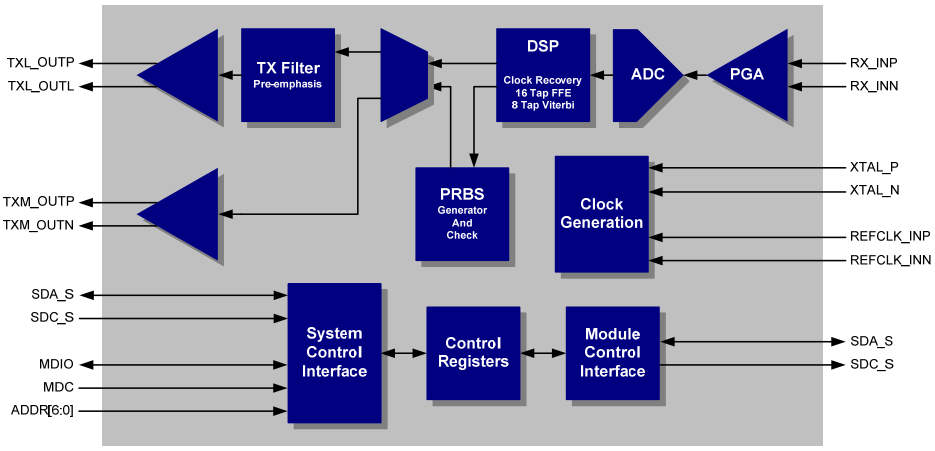

Figure 2, CL1012 Block Diagram

For more information on ClariPhy's products please visit our website www.clariphy.com or contact us at info@clariphy.com.

7585 Irvine Center Dr., Suite 100, Irvine, CA 92618 – phone +1 949 861-3074